

FORM HD-1449 (Based on Form PTO-1449)

**PATENT AND TRADEMARK OFFICE  
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Sheet 1 of 2

ATTORNEY DOCKET NO.

MP0088

SERIAL NO.

09/920,241

APPLICANT

Roo, Piete

FILING DATE

August 1, 2001

GROUP

2682

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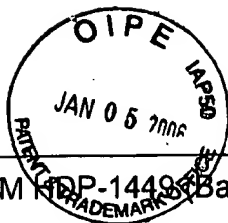
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2.	ef	WO 00/28663 A2	5/2000	Hatamian et al	—		
3.	ef	WO 00/28663 A3	5/2000	Hatamian et al	—		
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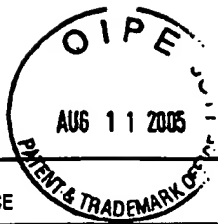
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## LIST OF REFERENCES CITED BY APPLICANT

APPLICANT

Pierte ROO

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Lin, et al., A 10-b, 500-Msample/s CMOS DAC in 0.6mm<sup>2</sup>

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	Lin, et al., A 10-b, 500-Msample/s CMOS DAC in 0.6mm <sup>2</sup>

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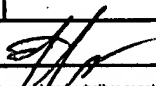
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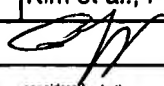


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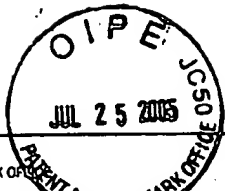
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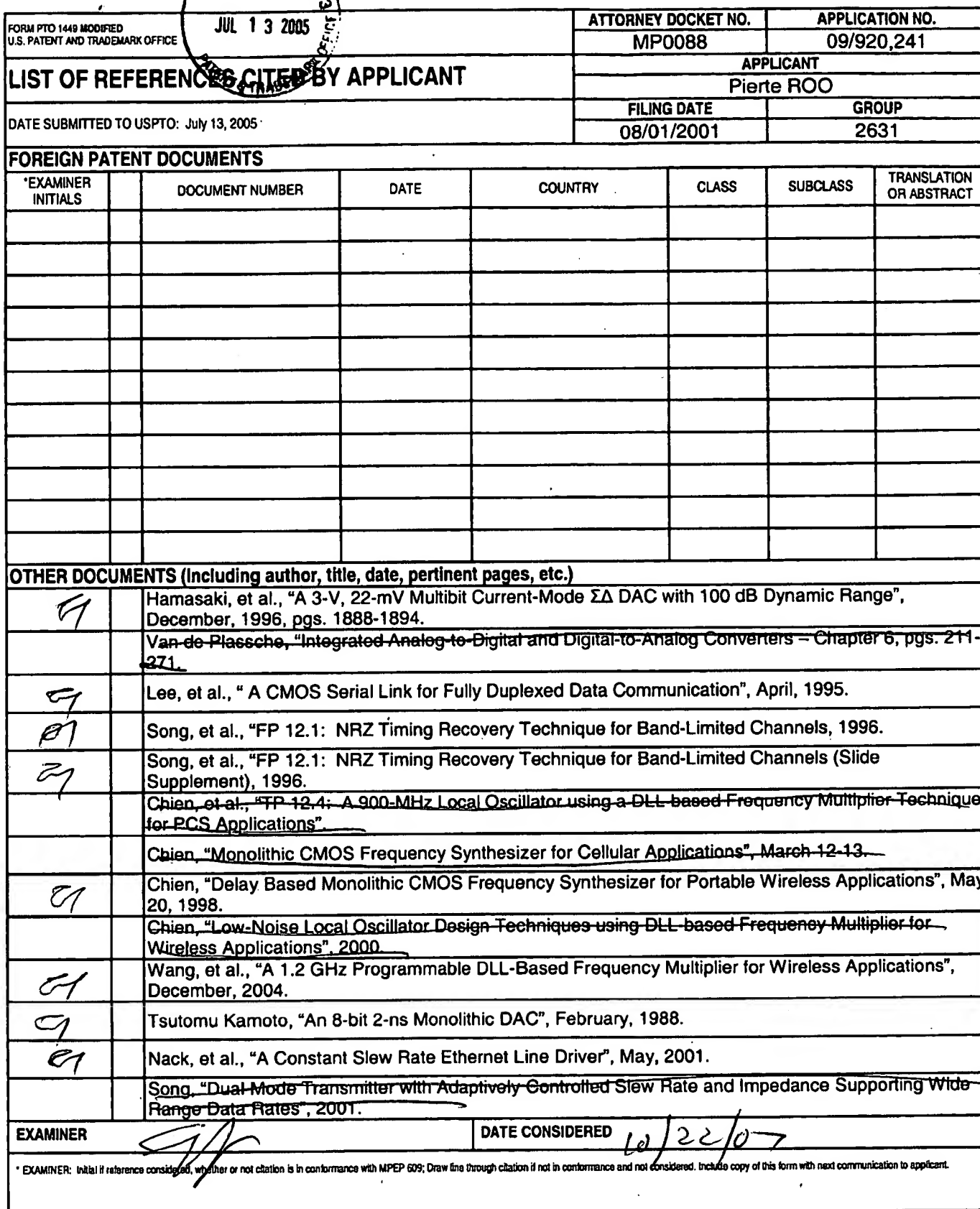


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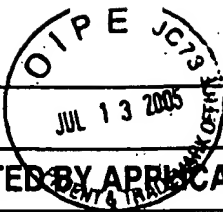
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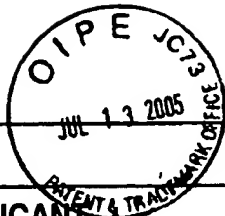
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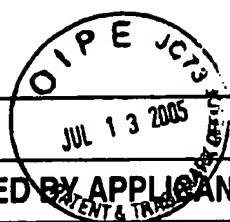
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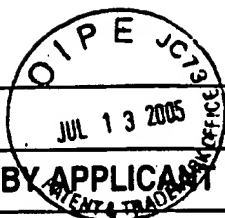
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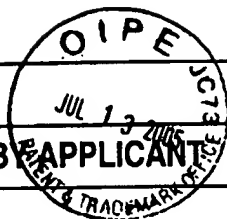
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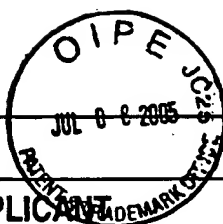
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MP0088

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09/920,241

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Pierre ROO

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